

FIG.1A

0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 0

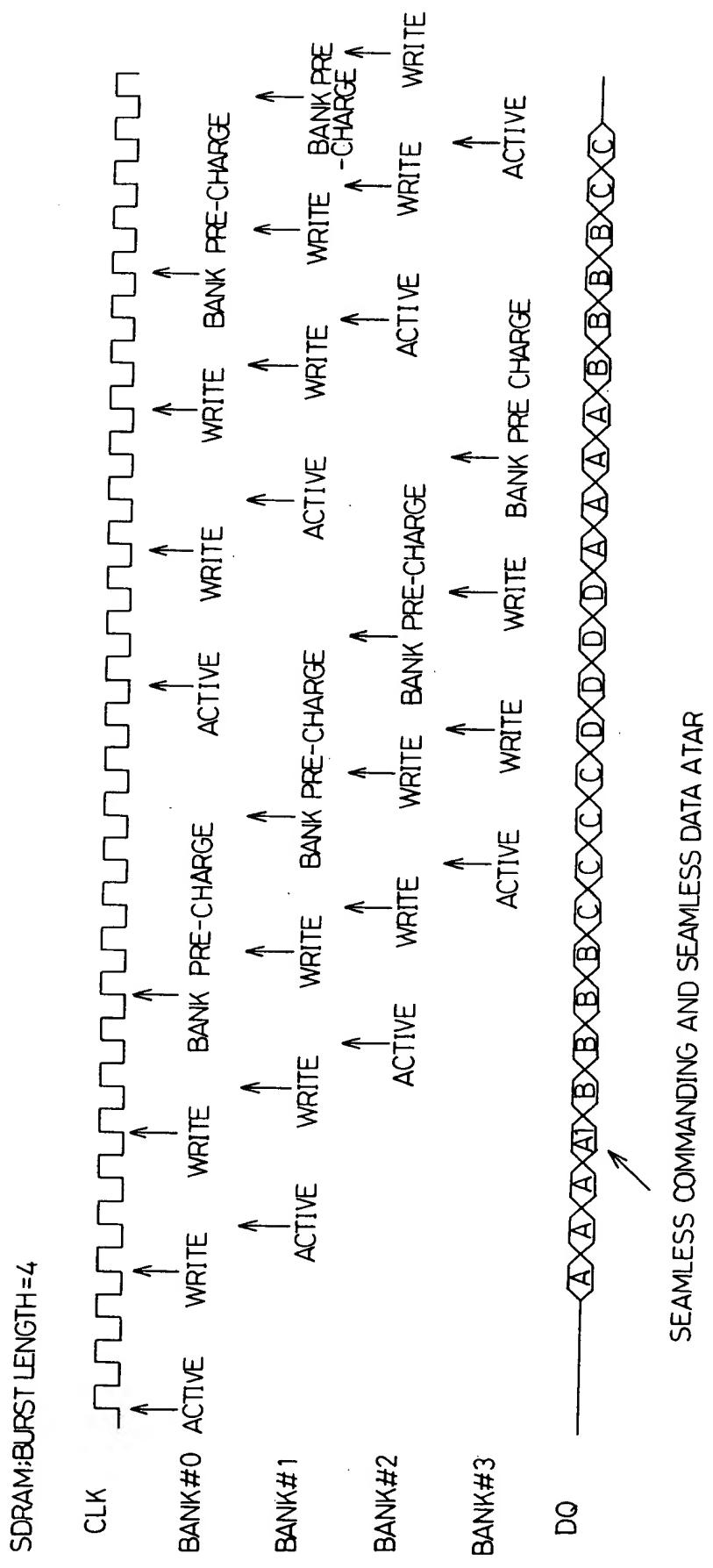


FIG.1B

SDRAM: BURST LENGTH=8

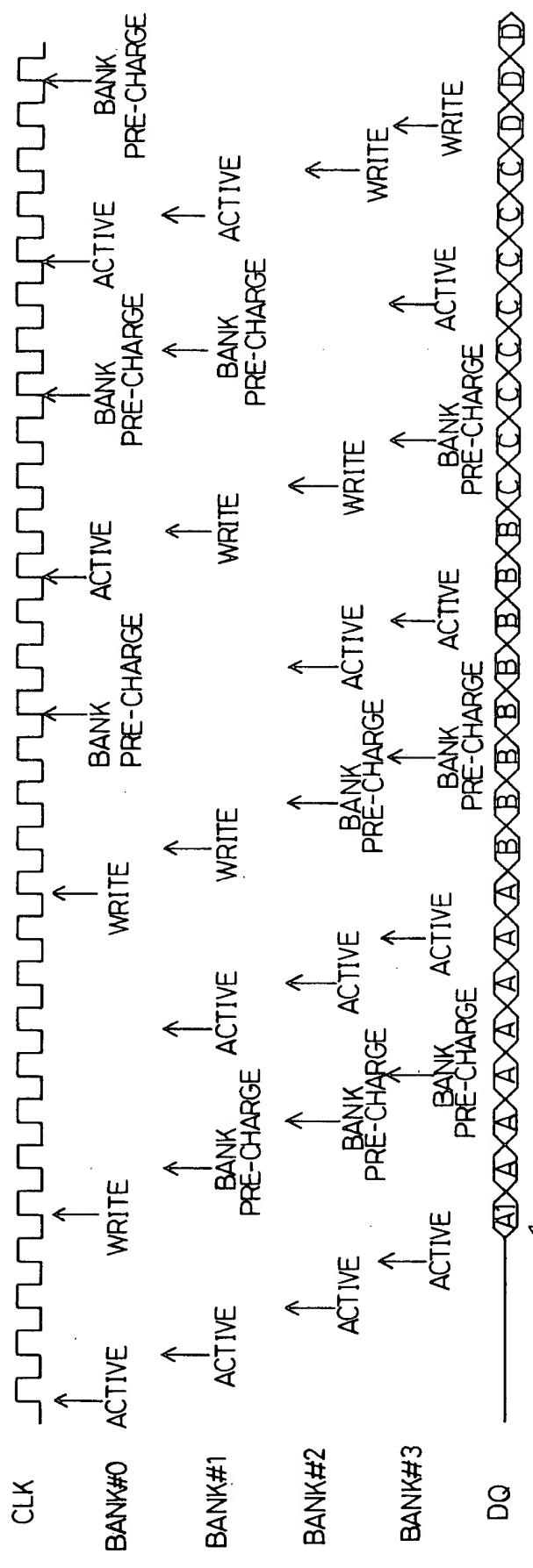


FIG. 1C

四庫全書

SDRAM;LATENCY=2;BURST LENGTH=2;

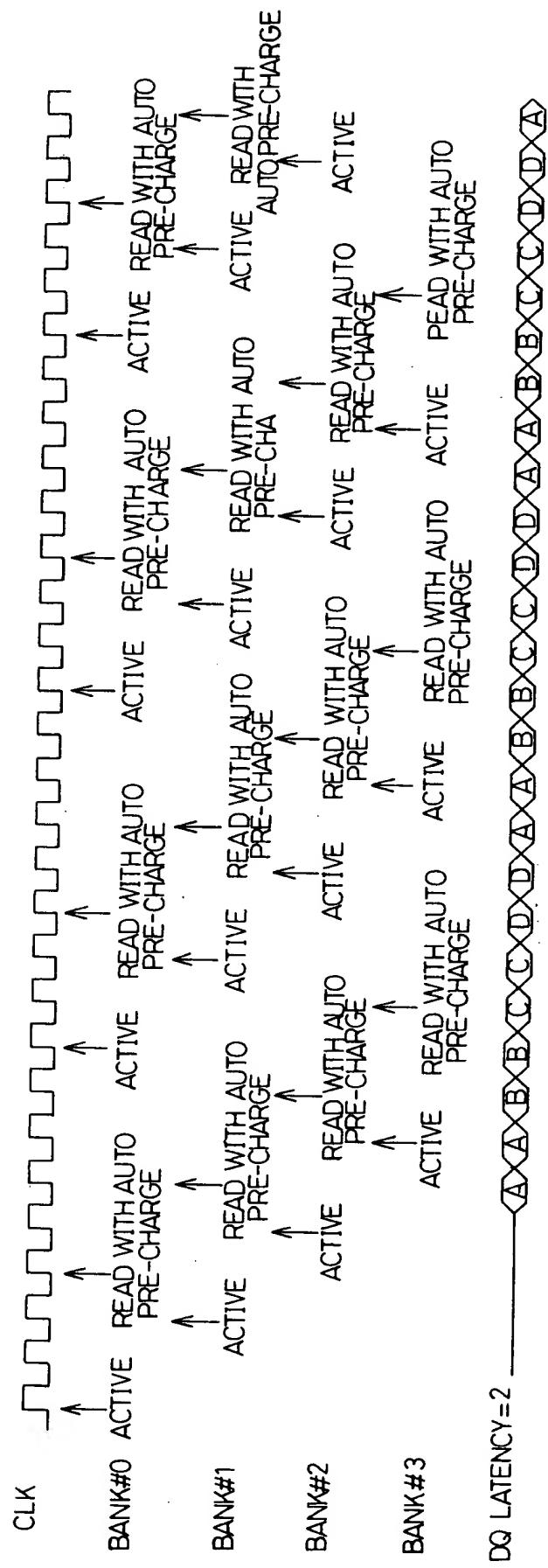


FIG. 2A

SDRAM:LATENCY=3:BURST LENGTH=2;

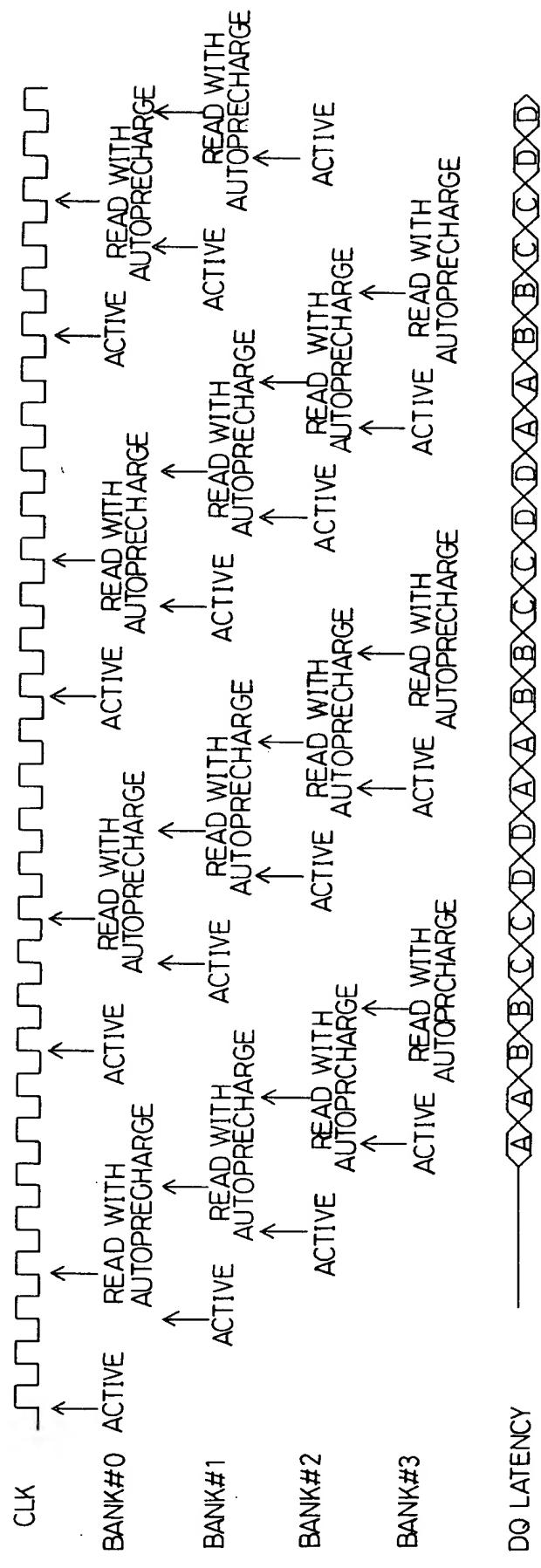


FIG. 2B

"F 0 T 2 S 0 " T h E S S S 6 0

SDRAM; BURST LENGTH=2

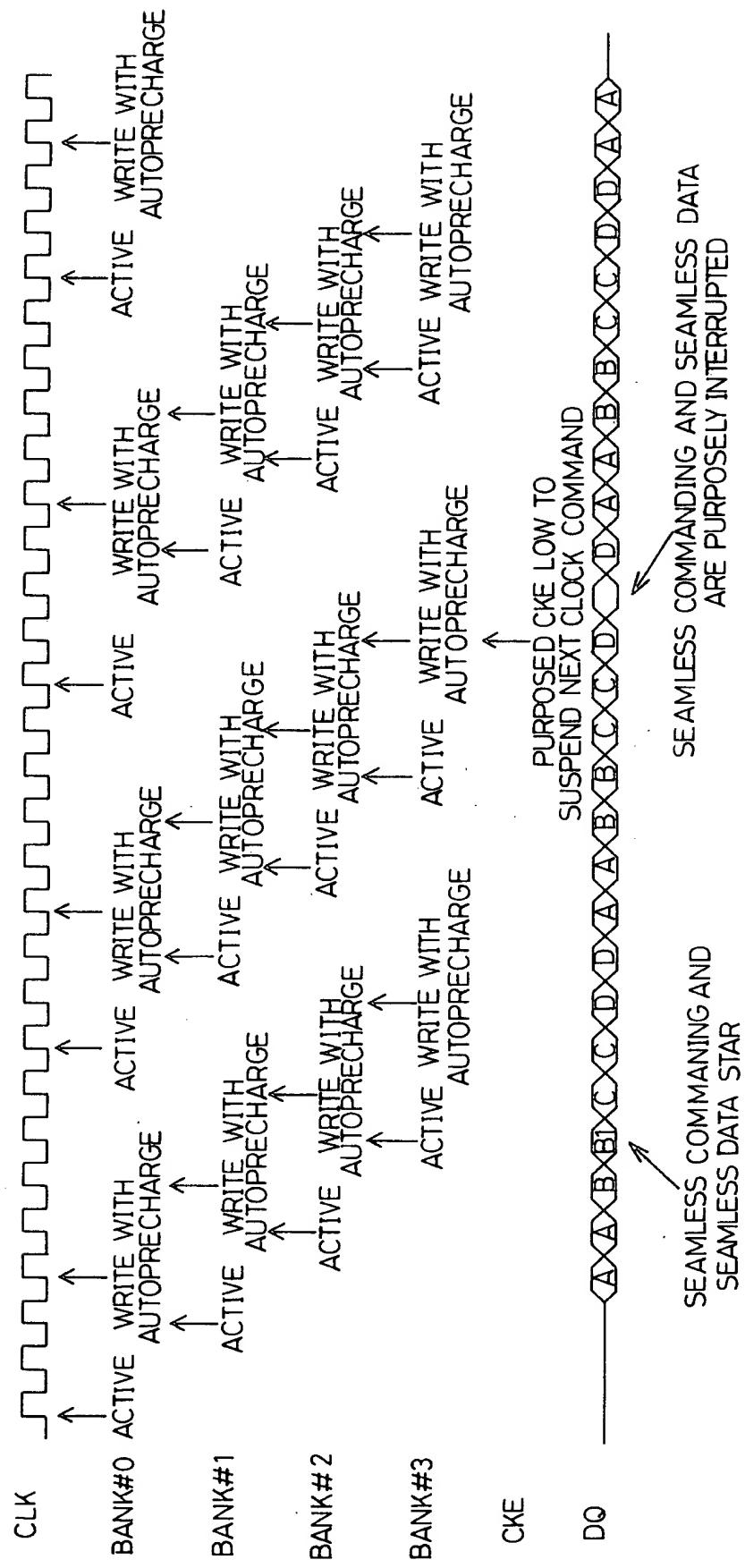


FIG. 2C

SDRAM: BURST LENGTH=2

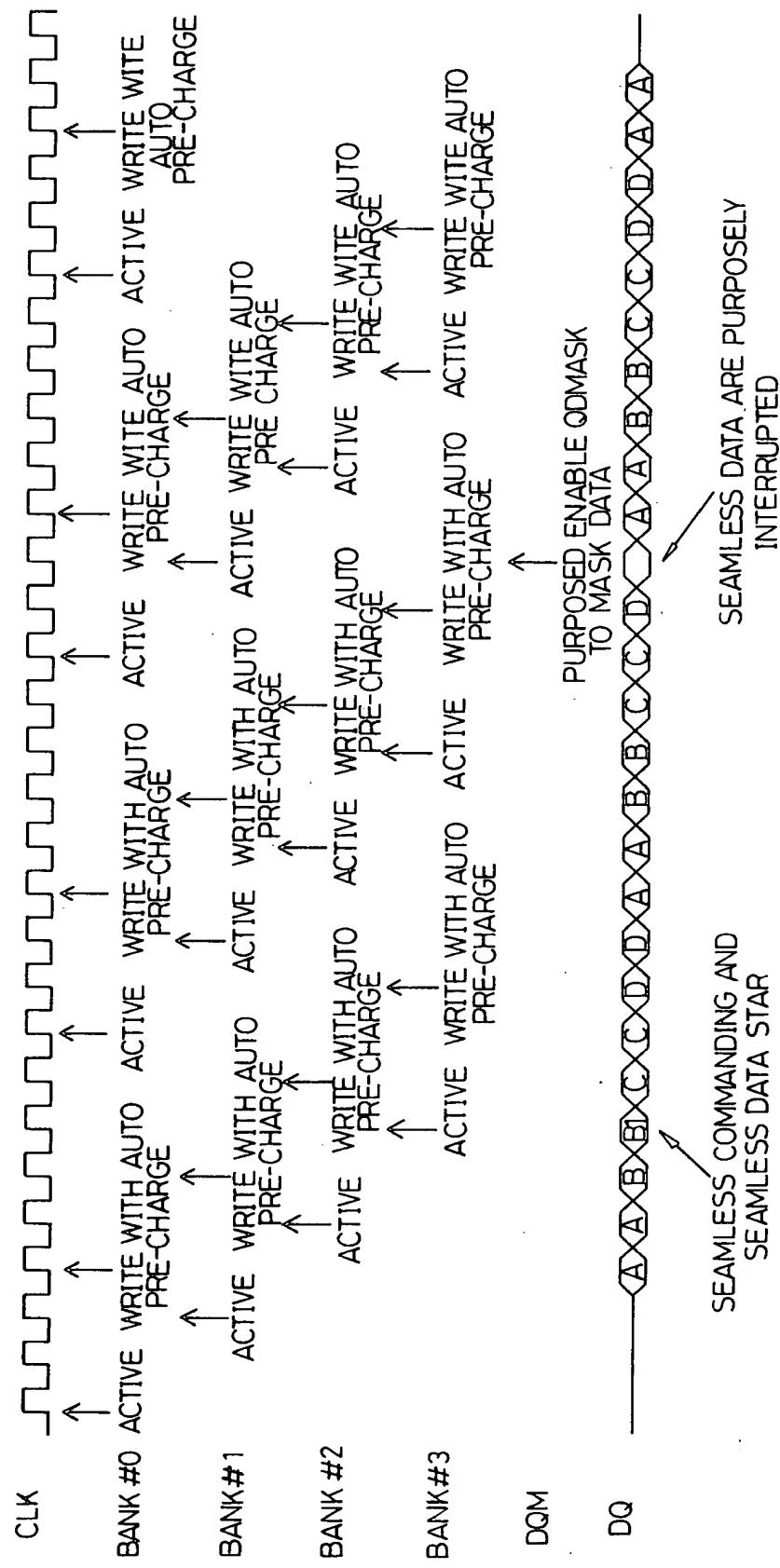


FIG. 2D

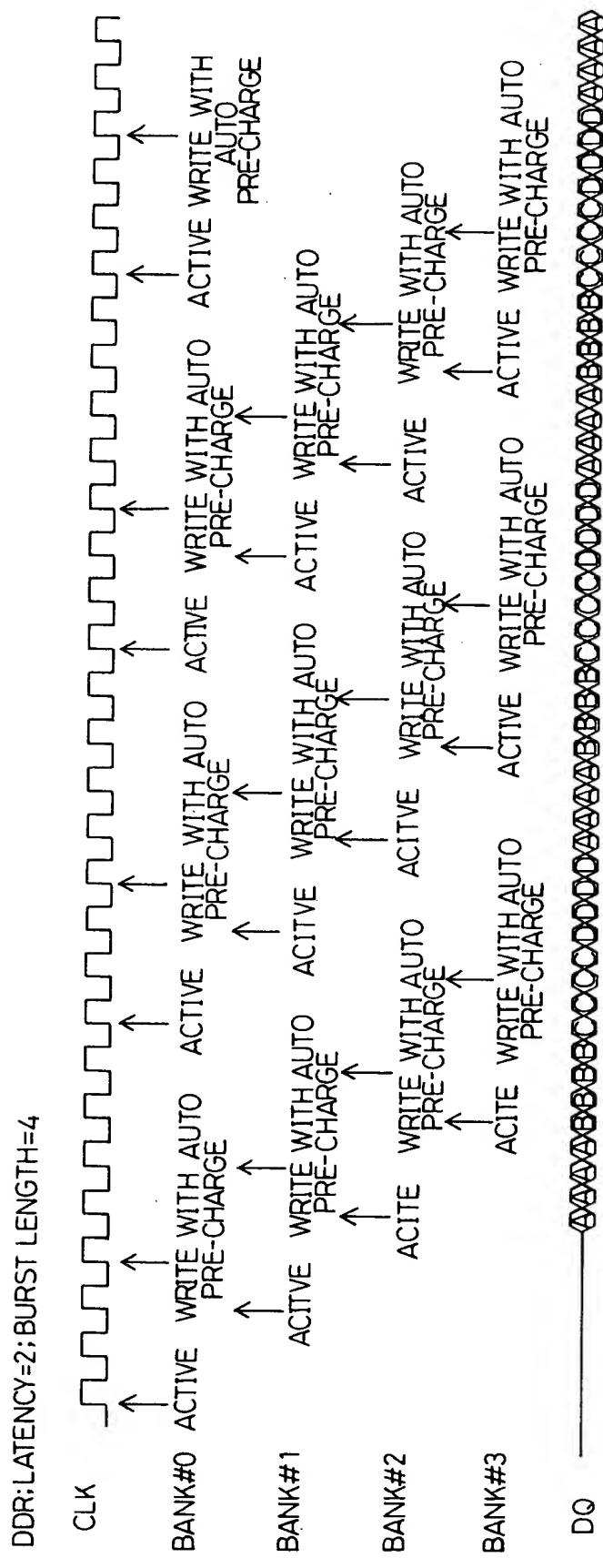


FIG. 3A

卷之三

DDR; LATENCY=2; BURST LENGTH=4

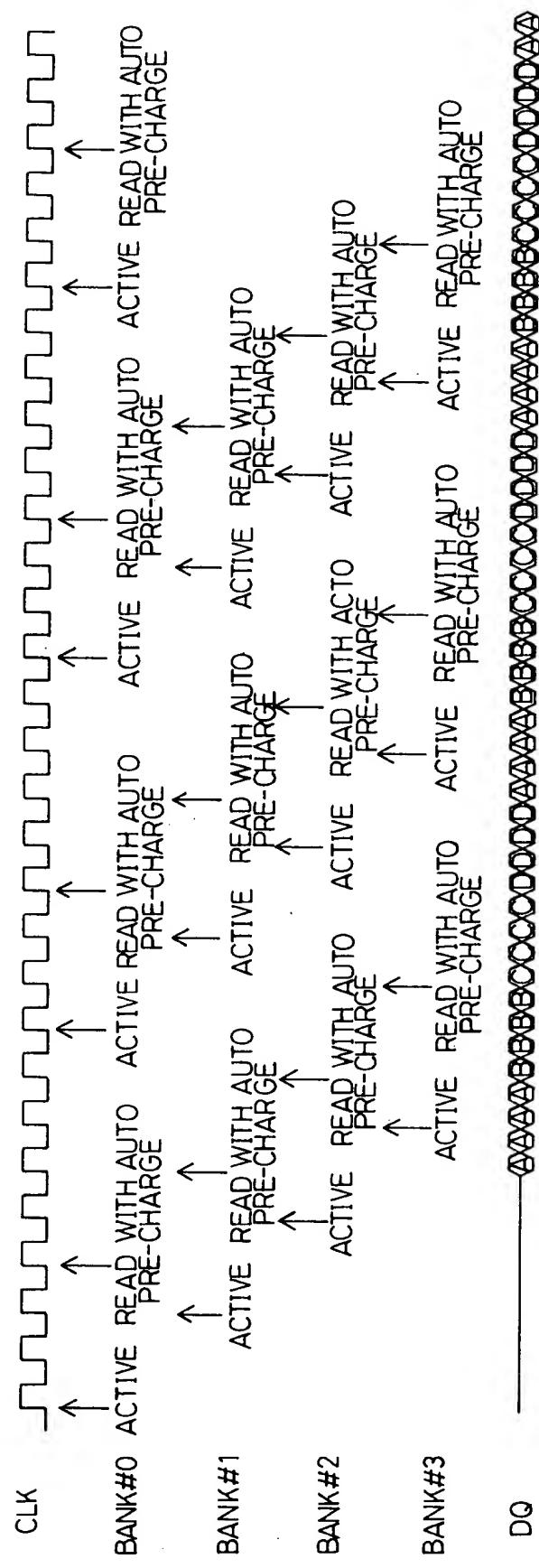


FIG. 3B

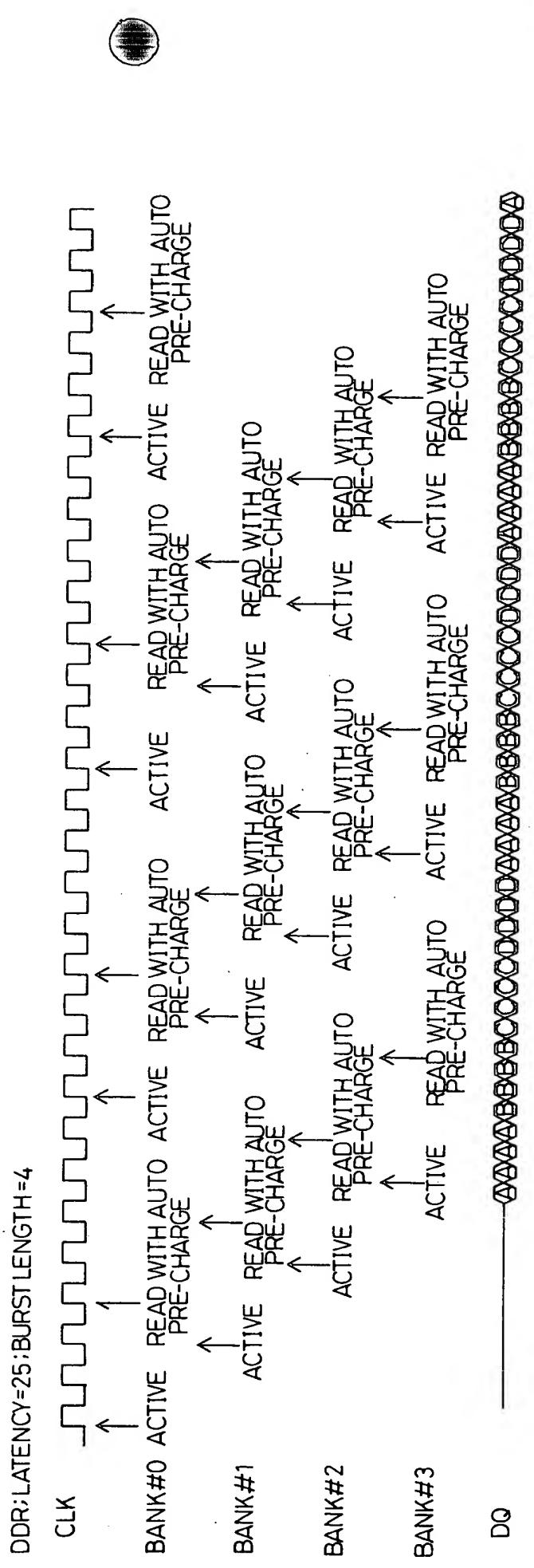


FIG. 3C

FIGURE 4.0 "FIGURE 4.0"

RDRAM: TRR=8 TCYCLE; TCWD=6 TCYCLE; TRTP=4 TCYCLE;

CTM' CFM' 

ROW2: (ACT a0) (ACT b0) (ACT c0) 

SEAMLESS COL PACKET COMMANDING →

COL4: (WR a1) (WR b1) (WR c1) (WR d1) (WR e1) (WR f1) (WR g1) (WR h1) (WR i1) (WR j1) (WR k1) (WR l1) (WR m1) (WR n1) (WR o1) (WR p1) (WR q1) (WR r1) (WR s1) (WR t1) (WR u1) (WR v1) (WR w1) (WR x1) (WR y1) (WR z1) 

SEAMLESS L.O. DATA PACKET →

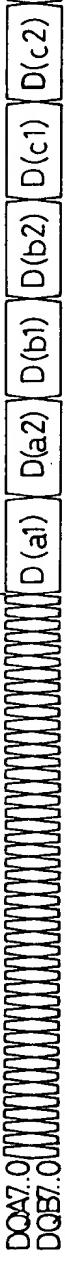
DQA7.0 (D(a1)) DQA7.1 (D(a2)) DQA7.2 (D(b1)) DQA7.3 (D(b2)) DQA7.4 (D(c1)) DQA7.5 (D(c2)) DQA7.6 (D(d1)) DQA7.7 (D(d2)) DQA7.8 (D(e1)) DQA7.9 (D(e2)) DQA7.10 (D(a3)) 

FIG. 4A

TRANSACTION A:	a0 = {Da, Ba, Ra0}	a1 = {Da, Ba, Ca1}	a2 = {Da, Ba, Ca2}	a3 = {Da, Ba, Ca3}	a4 = {Da, Ba, Ca4}
TRANSACTION B:	b0 = {Db, Bb, Rb0}	b1 = {Db, Bb, Cb1}	b2 = {Db, Bb, Cb2}	b3 = {Db, Bb, Cb3}	b4 = {Db, Bb, Cb4}
TRANSACTION C:	c0 = {Dc, Bc, Rc0}	c1 = {Dc, Bc, Cc1}	c2 = {Dc, Bc, Cc2}	c3 = {Dc, Bc, Cc3}	c4 = {Dc, Bc, Cc4}
TRANSACTION D:	d0 = {Dd, Bd, Rd0}	d1 = {Dd, Bd, Cd1}	d2 = {Dd, Bd, Cd2}	d3 = {Dd, Bd, Cd3}	d4 = {Dd, Bd, Cd4}
TRANSACTION E:	e0 = {De, Be, Re0}	e1 = {De, Be, Ce1}	e2 = {De, Be, Ce2}	e3 = {De, Be, Ce3}	e4 = {De, Be, Ce4}

RDRAM:TRR=8 TCYCLE;TCAC=8 TCYCLE;TRAS=20 TCYCLE;TRDP=4 TCYCLE;



ROW2..
ROW0.. {ACT a0} {ACT b0} {ACT c0} {PRER a0} {ACT a0} {PRER b0} {ACT a0} {PRER c0} {ACT a0} {PRER b0} {ACT a0} {PRER c0}

COL4..
COL0.. {RD a1} {RD a2} {RD b1} {RD b2} {RD c1} {RD c2} {RD d1} {RD d2} {RD a3} {RD d3} {RD b3} {RD d4} {RD c3}

DOAZ..
DQB7.. {D (a1)} {D (a2)} {D (b1)} {D (b2)} {D (c1)} {D (c2)} {D (d1)} {D (d2)} {D (a3)} {D (a4)}

FIG. 4 B

SDRAM: BURST LENGTH=4

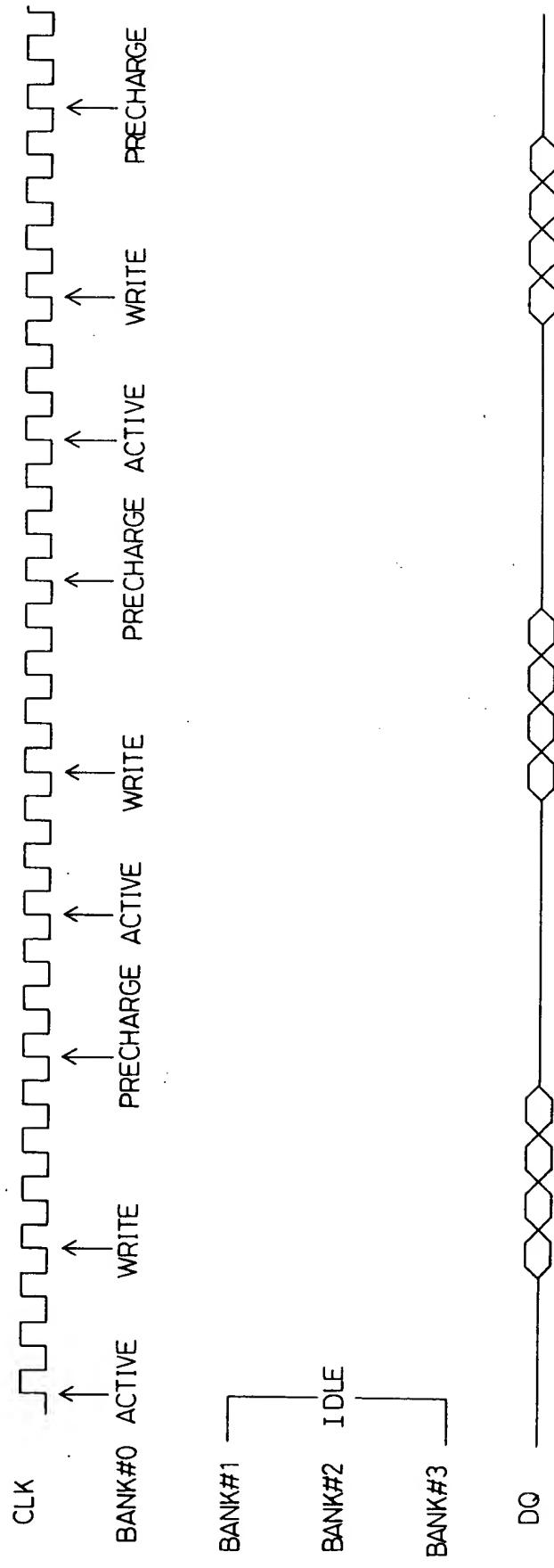


FIG. 5
PRIOR ART

“T 0 T 2 E 0 “ T 1 E 0 T 2 E 0

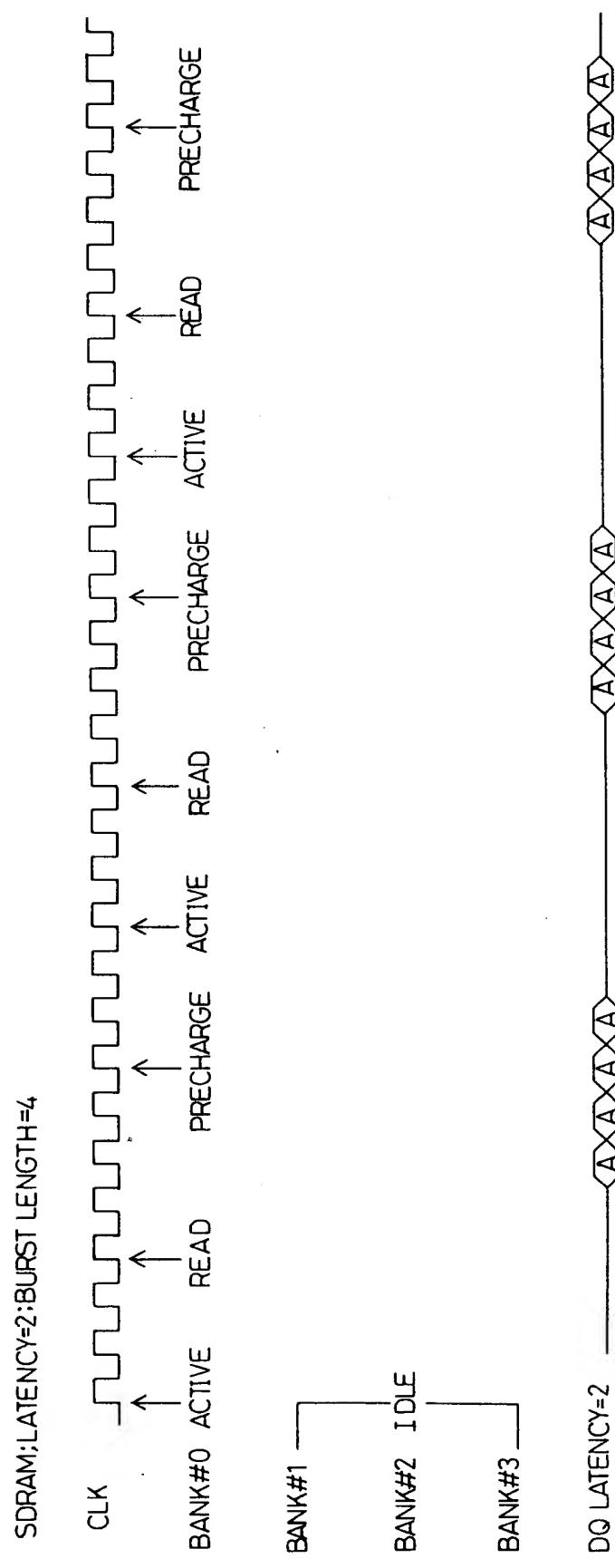


FIG.6A
PRIOR ART

“FIFO 230” FIFO 230

SDRAM; LATENCY=3; BURST LENGTH=4

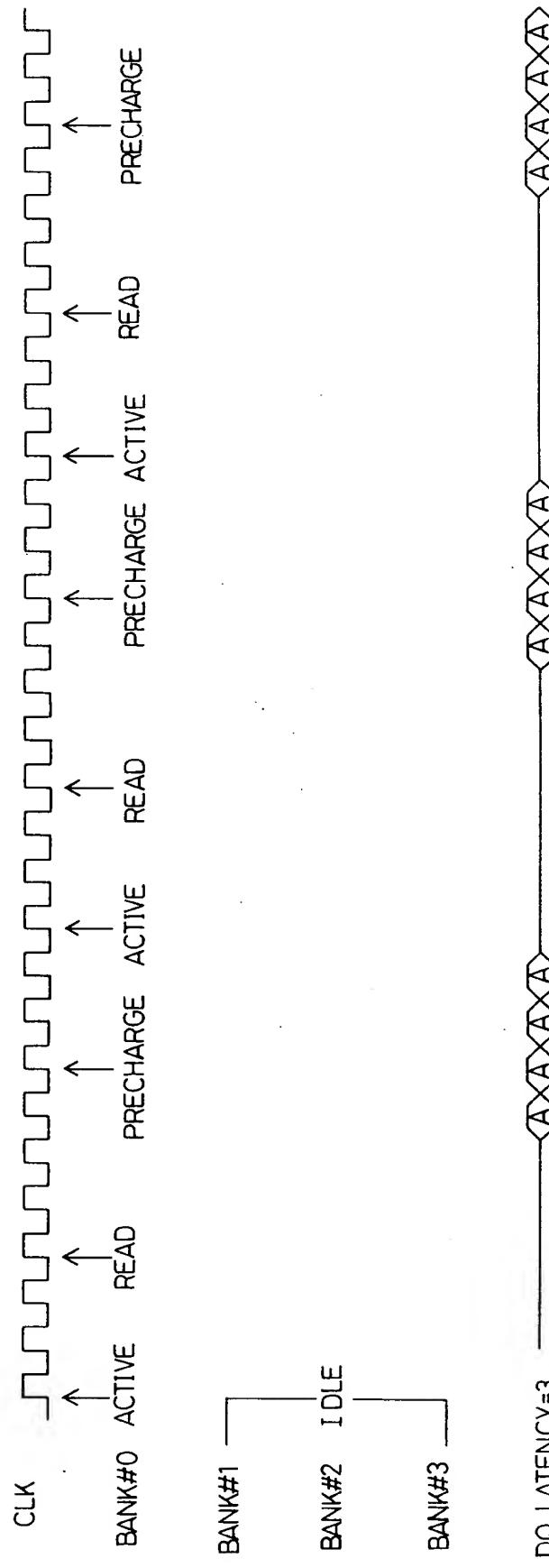


FIG.6B
PRIOR ART

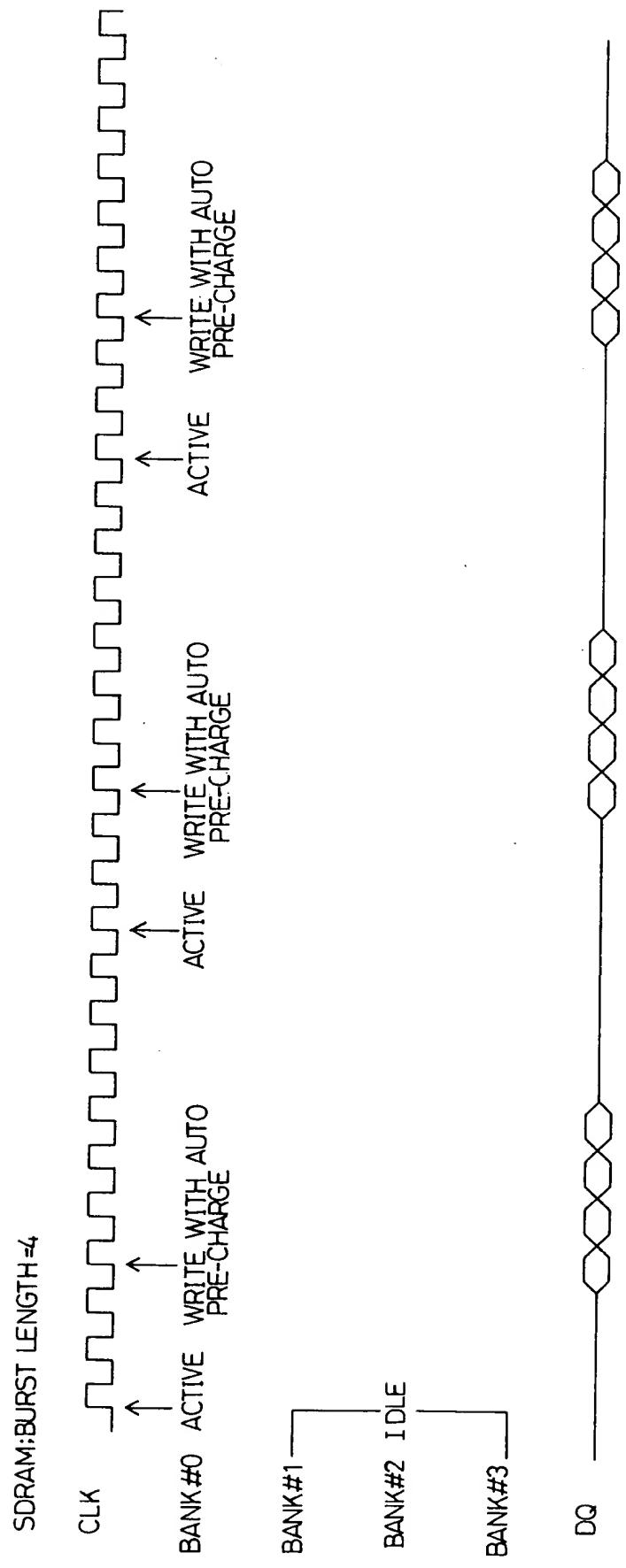


FIG. 7
PRIOR ART

FIGURE 8A

SDRAM;LATENCY=2;BURST LENGTH=4

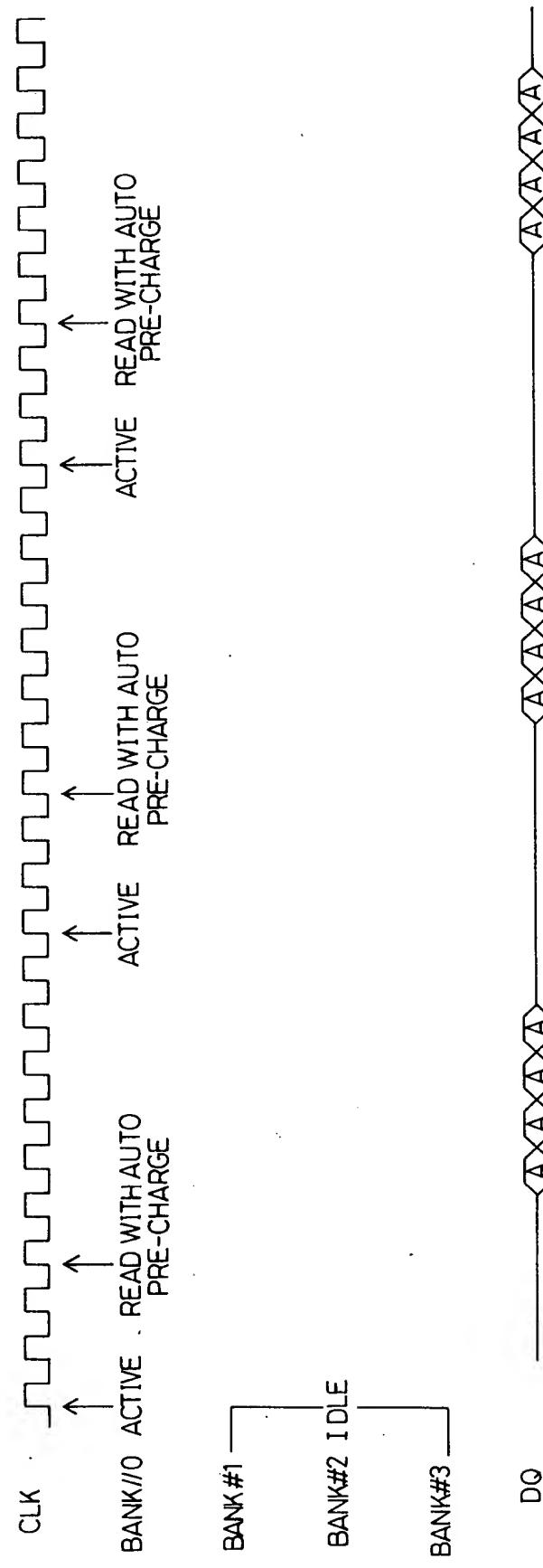


FIG. 8A
PRIOR ART

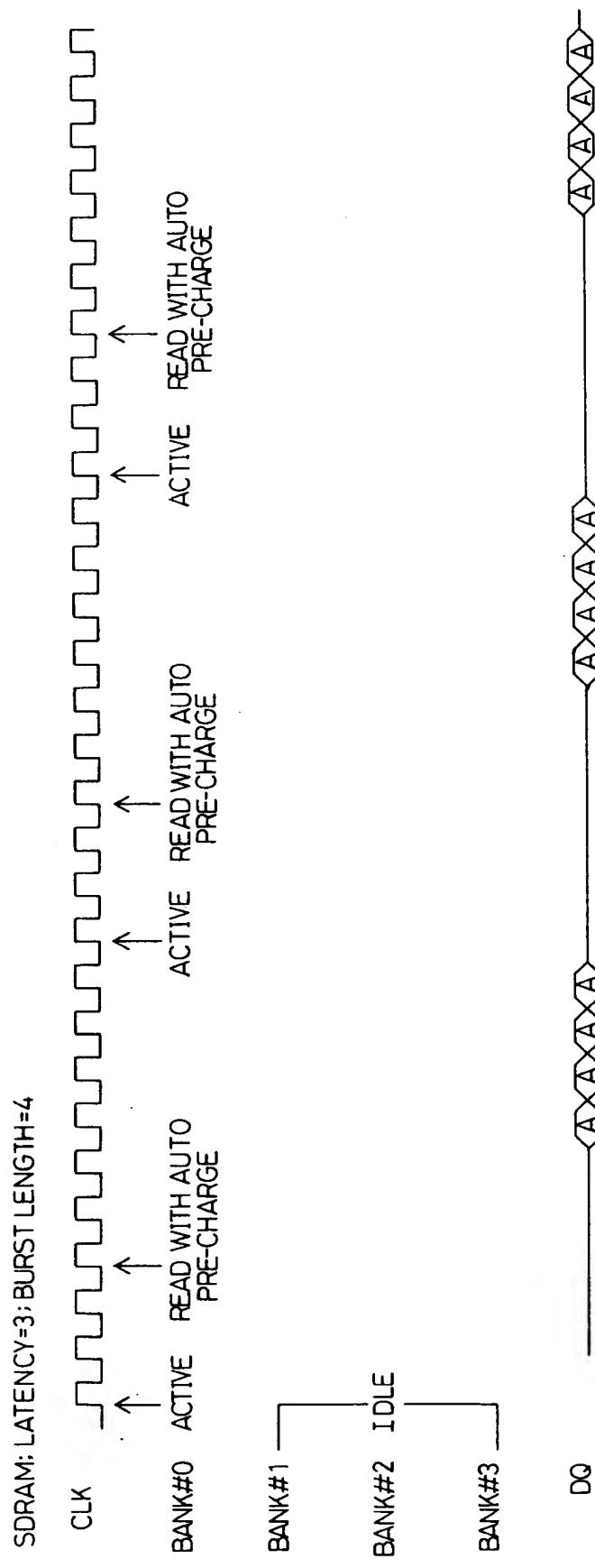


FIG. 8B
PRIOR ART

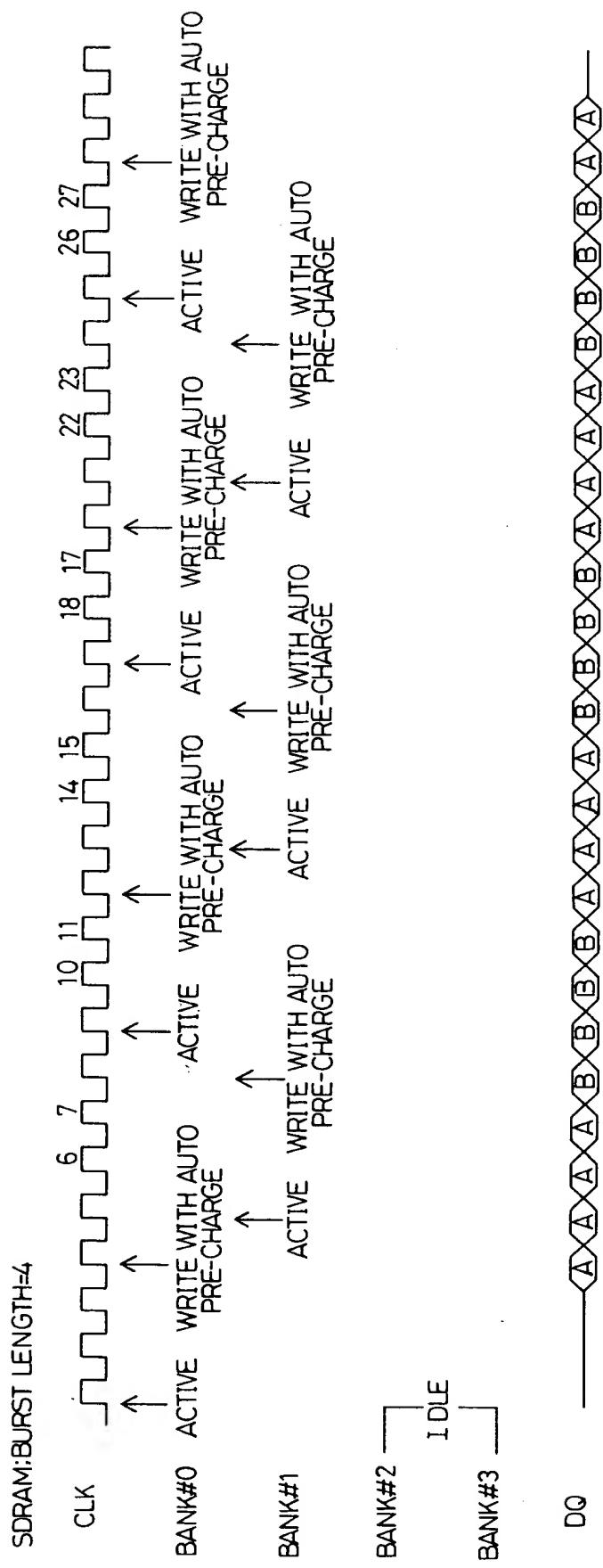


FIG. 9
PRIOR ART

卷之三

SDRAM: LATENCY=2; BURST LENGTH=4

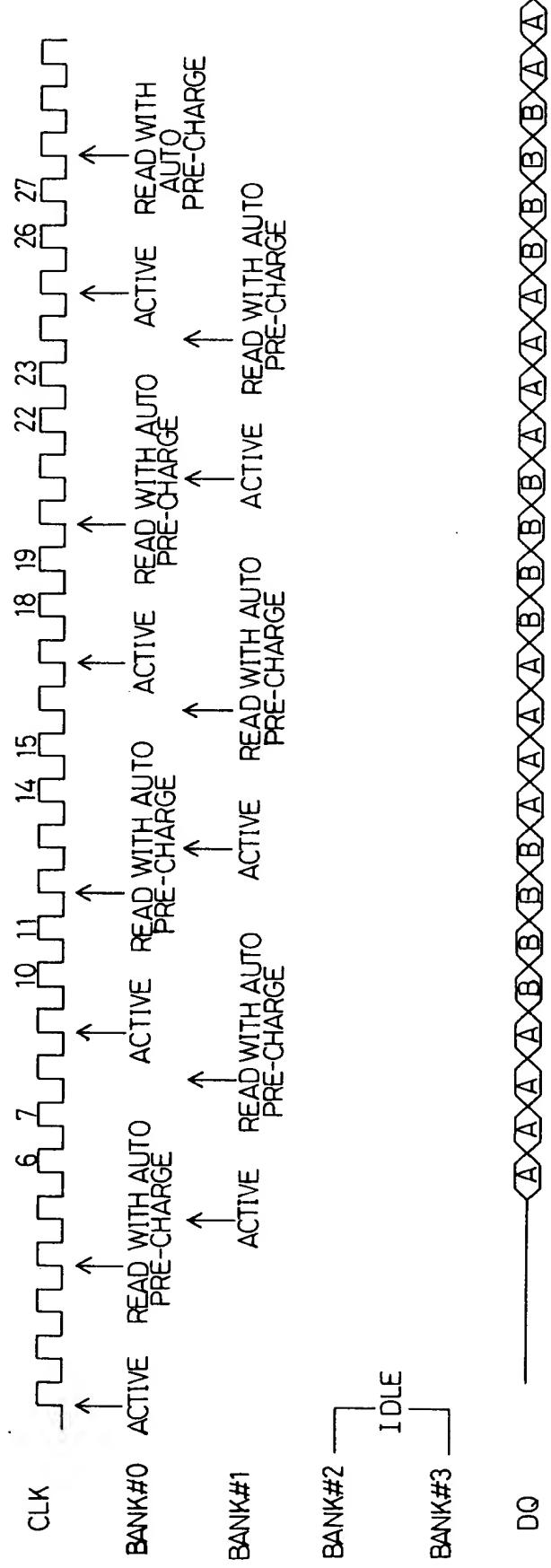


FIG. 10A PRIOR ART

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SDRAM:LATENCY=3; BURST LENGTH=4

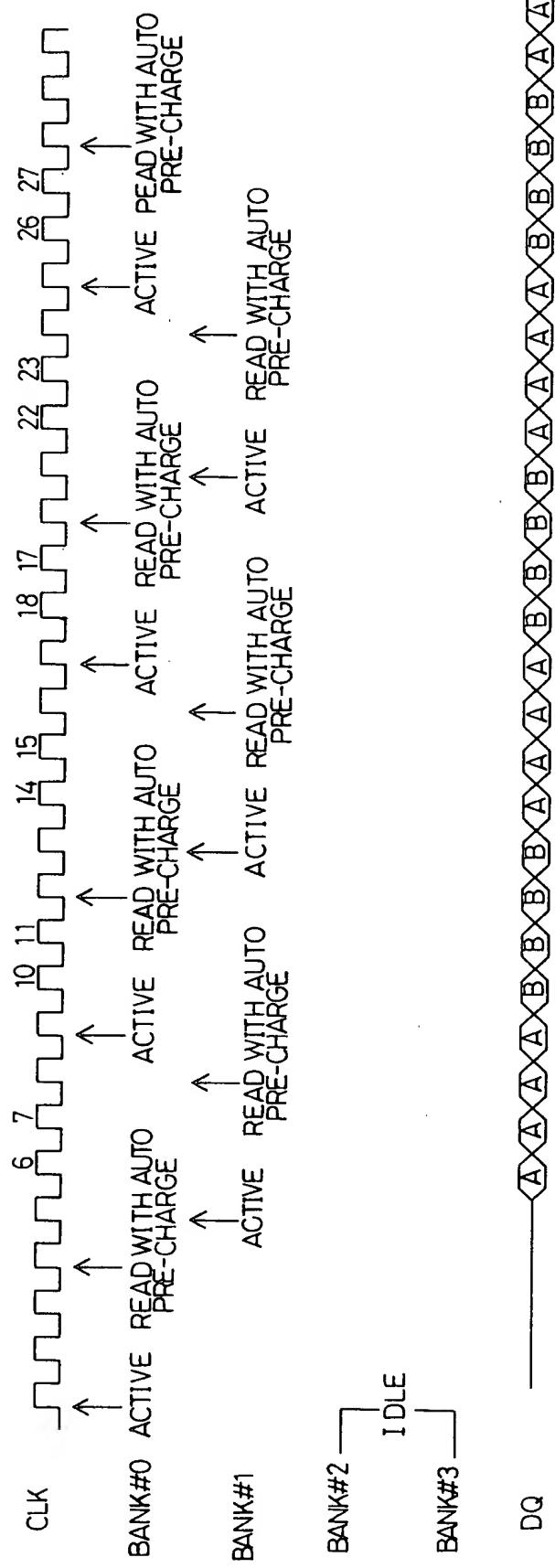


FIG. 10B
PRIORITY

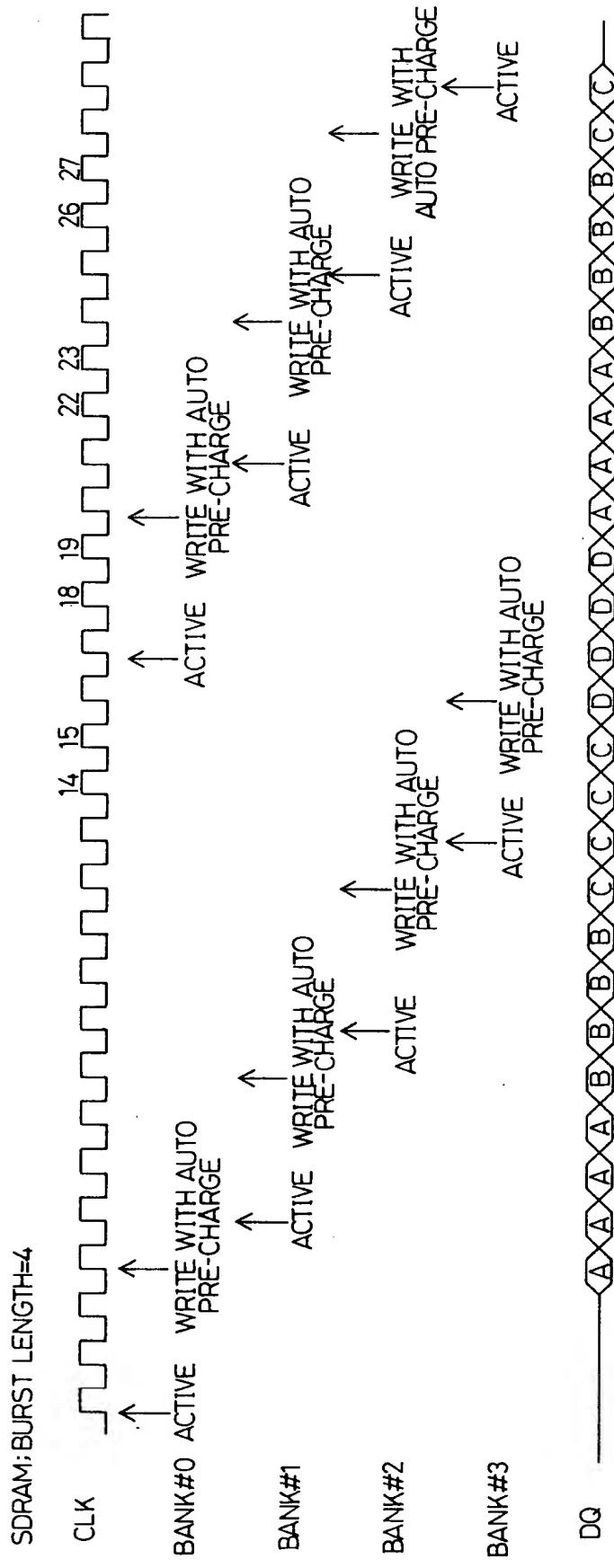


FIG.11
PRIOR ART

SDRAM;LATENCY=2;BURST LENGTH=4

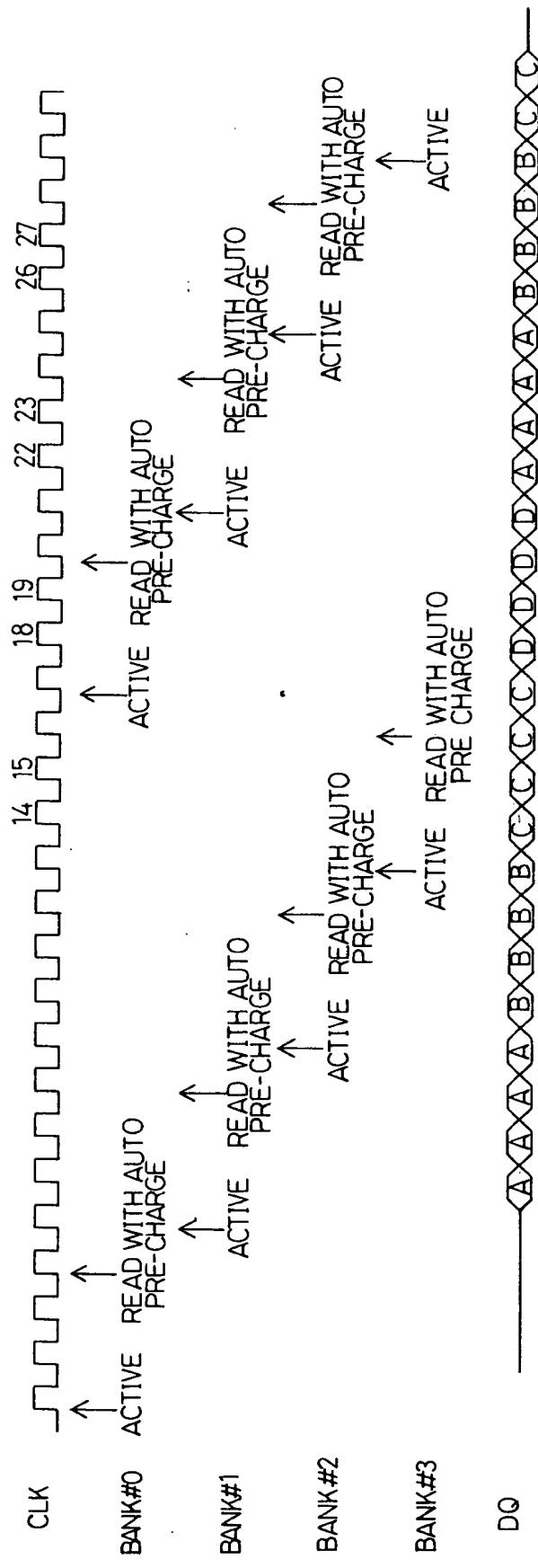


FIG. 12A
PRIOR ART

SDRAM: LATENCY=3; BURST LENGTH=4

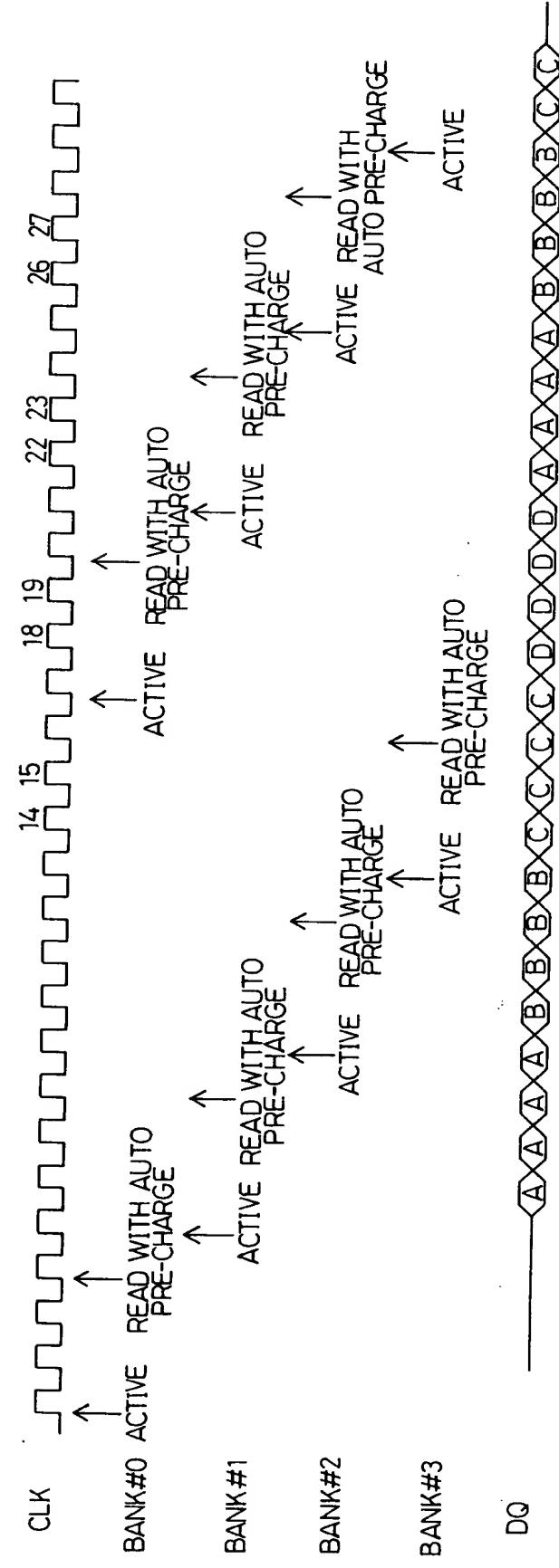


FIG.12B
PRIOR ART